REMARKS

Reconsideration of the above-referenced application in view of the above amendment, and of the following remarks, is respectfully requested.

Claims 1-14 are pending in this case. Claims 1 and 10 are amended herein.

The Examiner rejected claims 1-14 under 35 U.S.C. §103(a) as being unpatentable over Jang et al. (U.S.6,019,906) in view of Grill et al. (US 6,140,226) and further in view of Chen et al. (U.S. 6,319,822).

Applicant respectfully submits that claim 1 is patentable over Jang in view of Grill and Chen as there is no disclosure or suggestion in the references of extending the via by selectively etching the intrametal dielectric layer, then depositing a BARC layer within the via, and then etching a trench in the intrametal dielectric layer, wherein at the conclusion of trench etching step the via extends through the interlevel dielectric layer. Jang teaches a hardmask for etching a dielectric layer. Jang teaches etching vias, but not depositing the BARC layer within the via and etching the trench, or the via extending through an interlevel dielectric layer after extending the via to the intrametal dielectric layer. Grill teaches a trench-first dual damascene process. While the end structure of a via in the interlevel dielectric and a trench in the intrametal dielectric is obtain. Grill forms them in a different manner than claimed. Grill etches the trench first, not the via and deposits a BARC layer in the trench, not via. After depositing the BARC layer, Grill etches the via in the interlevel dielectric, but does not etch the trench in the intrametal dielectric as claimed, since the trench has been previously etched. Therefore, Grill does not disclos or suggest depositing a BARC layer within the via and then etching a trench in the intram tal dielectric

layer, wherein at the conclusion of trench etching step the via extends through the interlevel dielectric layer. Chen teaches a thicker barrier layer 52 in a via. The barrier layer comprises TiN which is a material that may be used as a BARC layer, although TiN layer 52 does not function as a BARC layer. The combination of the references does not disclose or suggest extending the via by selectively etching the intrametal dielectric layer, then depositing a BARC layer within the via, and then etching a trench in the intrametal dielectric layer, wherein at the conclusion of trench etching step the via extends through the interlevel dielectric layer, Accordingly, Applicant respectfully submits that claim 1 and the claims dependent thereon are patentable over the references.

Applicant respectfully submits that claim 4 is patentable over the references as there is no disclosure or suggestion in the references of the BARC layer filling the via to a level approximately even with the height of the interlevel dielectric layer. While the barrier layer of Chen may be thicker than that over the dielectric, there is no disclosure of filling the via to a level even with the height of the interlevel dielectric layer.

Applicant respectfully submits that claim 10 is patentable over the references as there is no disclosure or suggestion in the references of extending the via by selectively etching the intrametal dielectric layer and the shelf layer, then depositing a BARC within the via, and then etching a trench in the intrametal dielectric layer, wherein the trench etching step further extends the via through the interlevel dielectric layer. As discussed above, Jang teaches etching vias, but not depositing the BARC layer within the via and etching the trench, or the via extending through an interlevel dielectric layer after extending the via to the intrametal dielectric layer. Grill etches the trench first, not the via and deposits a BARC layer in the trench, not via. After depositing the BARC layer, Grill etches the via in the interlevel dielectric, but does not etch the trench in the intrametal dielectric as claimed, since the tr nch has been previously etched. Chin teaches a thicker TiN barrier layer 52 in a via. Thi combination of

the references do a not disclos or suggest extending the via by selectively etching the intrametal dielectric layer and the shelf layer, then depositing a BARC within the via, and then etching a trench in the intrametal dielectric layer, wherein the trench etching step further extends the via through the interlevel dielectric layer. Accordingly, Applicant respectfully submits that claim 10 is patentable over the references.

Claim 11 requires extending the via by selectively etching the intrametal dielectric layer and the interlevel dielectric layer. The BARC layer is deposited within the via and the trench is etched.

Applicant respectfully submits that claim 11 is patentable over the references as there is no disclosure or suggestion in the references of extending the via by selectively etching the intrametal dielectric layer and the interlevel dielectric layer and then depositing a BARC layer over the hardmask and within the via. As discussed above, Jang teaches etching vias, but not depositing the BARC layer within the via and etching the trench, or the via extending through an interlevel dielectric layer and an intrametal dielectric layer. Grill only teaches etching the top (Intrametal) dielectric before forming the thin conformal liner. Grill does not etch the via through both the intrametal dielectric and the intrametal dielectric. Grill etches the trench first, therefore the trench etch does not remove a portion of the BARC layer. Even if the terms trench and via are interchanged, the claim limitations are not met. Neither the trench or via is extended by selectively etching both the interlevel dielectric and the intrametal dielectric. Accordingly, Applicant respectfully submits that claim 11 and the claims dependent thereon are patentable over the references.

In light of the above, Applicant respectfully requests withdrawal of the Examiner's rejections and allowance of claims 1-14. If the Examiner has any questions or other correspondence regarding this pplication, Applicant requests

that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,

√acqueline J. Garner Reg. No. 36,144

Texas Instruments Incorporated P.O. Box 655474, M/S 3999 Dallas, TX 75265

PHONE: 214-532-9348 FAX: 972 917-4418